JOYDEEP BHATTACHARYYA

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PROFILE SUMMARY

- ASIC verification engineer with more than 11 years of experience including several successful tapeouts of multi-million gate ASICs.
- Worked with packet processing engines, network switches, PCI express, instruction caches, memory controllers.
- Extensive research experience in image processing, medical imaging, sensor signal processing
- Highly motivated and a great team-player with varied experience in handling collaborative work within a diverse workforce and across geographical locations.

TECHNICAL EXPERTISE

HDL	: Verilog
HVL	: UVM, System Verilog, Specman e
Simulation tools	: VCS, NC Verilog, Modelsim
Modeling languages	: SystemC
Programming Languages	: C, C++
Scripting skills	: Perl, Shell
Operating Systems	: UNIX, Linux, Windows XP

INDUSTRY EXPERIENCE

Company: Intel Corporation (101 Innovation Dr, San Jose, CA-95134)
Duration of work: May 2016 – Present
Hours per week: 40
Job Description: Working as a Senior Design Verification Engineer in Intel's next generation state-of-the-art networking chipsets. Responsibility includes taking active role in defining/implementing verification methodologies and modeling architectural specifications for performance analysis. Also taking leadership in defining the assertion based verification methodologies for the project.

Company: Ericsson Inc. (250 Holger Way, San Jose, CA-95134)
Duration of work: Sept 2014 -May 2016
Hours per week: 40
Job Description: Worked as a Senior ASIC Verification Engineer in the NPU team. Owned the verification of a complex cluster switching block connecting CPU and a network-on-chip (the block contained an instruction cache, hardware queues and temporary packet header storage). Also took active role in verification reviews of other blocks, mentoring junior engineers with coverage/assertion based testing and discussing/sharing ideas to improve verification quality.

- **Verification of cluster switching block:**
  - Created the verification plan, built a UVM testbench, created checkers, wrote and debugged all testcases.
  - Meticulously worked with designers/architects to improve the quality of verification, to eliminate possibility of late bugs
  - One of the first few members of the team to do extensive functional coverage based testing

Company: Juniper Networks Inc. (1194 N. Mathilda Ave, Sunnyvale, CA-94089)
Duration of work: June 2008 – Sept 2014
Hours per week: 40
Job Description: Owned several block/subsystem/chip testbenches for networking ASICs, with many first-time-working -silicon successes. Was also actively involved in verification experiments/ improvements, with other DV enthusiasts.

- **Memory subsystem verification (Oct 2012 – Sept 2014):** Successfully completed the verification of a critical block working with an architect and three designers while being the only DV engineer, built UVM testbench, implemented constrained random testcases, System Verilog Assertions, code and functional coverage, assisted in related full-chip debug
- **Several block and chip level verification tasks (Mar 2010-Sept 2012):** Testplan documentation, SystemC/SV/UVM testbench creation, testcase writing and debug, closing on coverage.
- **Verification of a complex queue-ing module (June 2008 – Feb 2010):** Quickly ramped up on SystemC and created a solid testbench infrastructure, was one of the first few engineers in the team in implementing newly adopted System Verilog Assertions and functional coverage methodologies. Found a critical bug with SVAs and finally delivered a bug-free silicon.

Company: Cisco Systems (725 Alder Dr., Milpitas, CA-95035)
Duration of work: May 2008 – June 2008
Hours per week: 40
Job Description: Worked on verification of a network processing FPGA.

- Improved an existing specman testbench from a previous generation to enable new features, developed the new testplan and wrote new perl based testcases and checkers/assertions.

Company: Intel India Technology Pvt Ltd (23-56P, Varthur Hobli, Outer Ring Road, Devarabisanahalli, Bengaluru, Karnataka 560103, India)
Duration of work: July 2005 – April 2008
Hours per week: 40
Job Description: Worked on RTL design and DVwith Intel's Graphics/chipset teams

- **Design/verification for instruction cache units of GPU:**
  - Design work involved micro-architectural changes, RTL coding and timing closure.
  - Verification included testbench/stimuli/checker development, testcase writing and assertions (specman). Also assisted in full-chip verification and post-silicon debug.
- **Verification of PCI express interfaces of Intel's north bridge chip:** Testplan creation/review, writing directed/random tests, enhancing the checkers/assertions, reproduce post-silicon bugs in RTL/gate simulation environment.

RESEARCH EXPERIENCE

A) Design and Development of an Embedded Ultrasound Imaging System:

- Setting up the system specification
- Design and analysis of algorithms for different modules of an ultrasound system
- Architectural design and FPGA implementation of the digital modules

B) Implementation of a real time noise cleaning algorithm to remove the speckle noise present in ultrasound echocardiographic images:

- Algorithm and architecture has been designed and implemented in Xilinx FPGA for the noise cleaning filter.
- A new sorter has also been proposed in the design.
- The module works with 115 frames/second and consumes a total of 106,567 gates.

C) Design and implementation of a CORDIC based real time scan conversion unit for ultrasound imaging:

- A combined interpolation scheme has been designed and developed.
- Also corresponding architecture has been realized in Xilinx FPGA.
- The architecture is suitably pipelined and parallelized in order to increase the throughput of the system.
- Total number of gate count is 1, 50,186.

D) Algorithm development and VLSI implementation of dynamic receive apodization unit for a digital delaysum beamformer:

- An algorithm has been proposed and implemented in Xilinx FPGA to enable real time dynamic receive apodization for an ultrasound beamformer.
- The design is based on pipelined CORDIC, works with 40 frames/s and consumes a total of 22,586 gates.

E) VLSI implementation of real time delay generation for a digital delay-sum beamformer:

- A delay value generation algorithm has been implemented in Xilinx FPGA which utilizes the Fresnel approximation scheme.
- Corresponding delay memory has been designed utilizing the BlockRAMs available in the device.

F) Design, Fabrication and Testing of a Porous Silicon Pressure Sensor:

- Designed a porous silicon based piezoelectric pressure sensor
- Designed the associated analog and digital signal processing part
- The sensor worked with full atmospheric pressure range
- The design was capable of correcting nonlinearities
- Also, the mathematical model was proposed for the pressure sensor

TEACHING EXPERIENCE

- Worked as a lecturer in Indian Institute of Information Technology, Kolkata, India during Sept 2001- March 2002
- Taught the following courses:
  - Signals and Systems Theory (Undergraduate, 2nd year)
  - Basic Electronics (Undergraduate, 1st year)

EDUCATIONAL QUALIFICATION

- **M.S. in Electronics & Electrical Engineering**
  - July 2003 – July 2005
  - Major in Very Large Scale Integration (VLSI) systems
  - From Indian Institute of Technology, Kharagpur (Kharagpur, West Bengal 721302, India)
  - CGPA 9.65/10
  - 2nd place among 45 students
  - Thesis title: "Design and Development of an Embedded Ultrasound Imaging System"
  - Advisor: Prof. Swapna Banerjee

- **B.E. in Electronics & Telecommunication Engineering**
  - August 1997 – June 2001
  - Major in electronics & Telecommunication Engineering
  - From Jadavpur University (188, Raja S.C. Mallick Rd, Kolkata, West Bengal 700032, India)
  - Marks obtained: 81.2 %
  - Thesis title: "Design of an OPAMP for a porous silicon sensor signal processing system"
  - Advisor: Prof. Hiranmay Saha

ACHIEVEMENTS

- Ericsson team recognition award for Gen4 NPU development
- Juniper networks CEO recognition award for contribution in developing Broadway platform
- Juniper networks CEO recognition award for contribution in developing Cassis 2 platform
- Intel recognition award for successful launch of Calistoga (Napa) platform (2006)
- Recognition award from President of Intel, India for successful launch of Santa Rosa platform (2007)
- Invited talk at Jadavpur University, India
- Secured second place among all M.S. students (CGPA: 9.65/10)
- Scholarship for Post Graduate Studies in Engineering, Indian Space Research Organization, 2003-2005
- Qualified Graduate Aptitude Test in Engineering (GATE) in 2002 (Percentile : 98.56 , All India Rank : 273 out of 40,000 students)
- Award and National Merit Scholarship from State Government of West Bengal, India for securing 8th position among nearly 400,000 students in 10+2 exam.
- Award and National Merit Scholarship from State Government of West Bengal, India for securing 13th position among nearly 500,000 students in 10th standard exam
- Rotary Club of Calcutta award for securing 1st position in the district in 10th standard exam

SELECTED COURSEWORKS

- Architectural design of IC
- Network Theory
- VLSI circuits and systems
- Discrete Electronic Circuits
- CAD of VLSI
- Digital Logic
- DSP and its applications
- Microprocessors (8085)

PUBLICATIONS

1. Real Time Noise Cleaning of Ultrasound Images, 17th IEEE Symposium on Computer-Based Medical Systems, Bethesda, Maryland, pp. 379-384, 24-25 June 2004. Co-author: A.Hazra and S. Banerjee.

2. A Real Time Speckle Noise Cleaning Filter for Ultrasound Images, 19th IEEE Symposium on Computer-Based Medical Systems, Salt Lake City,Utah, June 22-23, 2006, Co-author. B. Mazumdar, A. Mediratta, S. Banerjee .

3. Architectural Design and Implementation of a PC based Ultrasound Imaging System, 10th IEEE VLSI Design and Test Symposium, Goa, India, 9-12 August 2006, Co-author: B. Mazumdar, A. Mediratta, S. Banerjee.

4. **Real Time Dynamic Receive Apodization for an Ultrasound Imaging System**, Proceedings of VLSI Design'2006. pp.534~537, Co-author: P.Mandal, R.Banerjee and S. Banerjee.

5. **Design, Fabrication, Testing and Simulation of Porous Silicon Based Smart MEMS Pressure Sensor**, 18th International Conference on VLSI Design and 4th International Conference on Embedded Systems, Kolkata, India, January 3-7, 2005. Co-author: C. Pramanik, T.Islam, H. Saha, S. Banerjee, S. Dey.

6. **A CORDIC Based Real Time Scan Conversion Unit for Ultrasound Imaging**, International Conference on Imaging, Beijing, China, May 23- 26, 2005. Co-author: Shayak Banerjee, Anindya hazra, Swapna Banerjee

7. **Real Time Dynamic Receive Apodization for an Ultrasound Imaging System**, 3rd International Conference on Computing, Communications and Control Technologies, July 24-27, 2005 , Austin, Texas, USA, Co-author: P.Mandal, R.Banerjee and S. Banerjee.

8. An Embedded System Design of Selective Window Speckle Noise Suppression Filter for Ultrasound Images , 1st International Conference on Industrial and Information Systems, Peradeniya , Srilanka, August 8-11, 2006. Co-author: B. Mazumdar , A. Mediratta , S. Banerjee .